Low-Voltage 1:9 Differential ECL/PECL Clock Driver

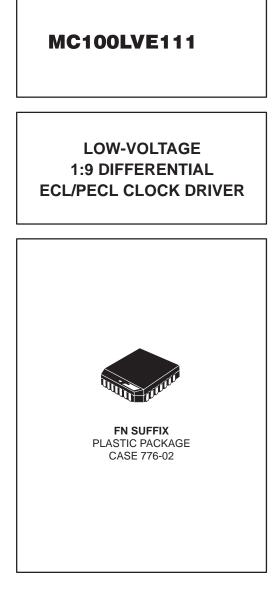
The MC100LVE111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the popular MC100E111, with the added feature of low voltage operation. It accepts one signal input, which can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs.

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage VEE Range of -3.0 to -3.8V
- 75kΩ Input Pulldown Resistors

The LVE111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determineprocess control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω , even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

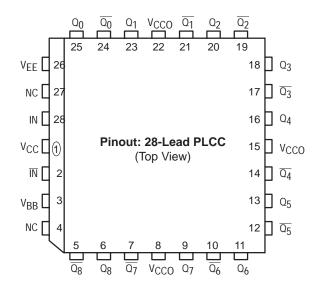
The MC100LVE111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For systems incorporating GTL, parallel termination offers the lowest power by taking advantage of the 1.2V supply as a terminating voltage. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.



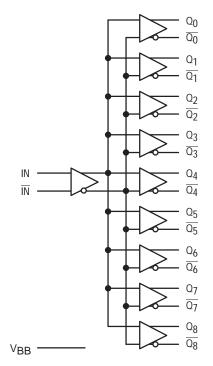
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PIN NAMES

Pins	Function
$\begin{matrix} \text{IN,} \ \overline{\text{IN}} \\ \text{Q}_0, \ \overline{\text{Q}_0} \text{-} \text{Q}_8, \ \overline{\text{Q}_8} \\ \text{V}_{\text{BB}} \end{matrix}$	Differential Input Pair Differential Outputs V _{BB} Output



LOGIC SYMBOL



ECL DC CHARACTERISTICS

			–40°C		0°C				25°C					
Symbol	Characteristic	Min	Тур	Max	Unit									
VOH	Output HIGH Voltage	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	V
V _{OL}	Output LOW Voltage	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	V
VIH	Input HIGH Voltage	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V
VIL	Input LOW Voltage	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	V
V _{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
VEE	Power Supply Voltage	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	V
Iн	Input HIGH Current			150			150			150			150	μΑ
IEE	Power Supply Current		55	66		55	66		55	66		65	78	mA

PECL DC CHARACTERISTICS

			–40°C			0°C			25°C					
Symbol	Characteristic	Min	Тур	Max	Unit									
VOH	Output HIGH Voltage ¹	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V _{OL}	Output LOW Voltage ¹	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
VIH	Input HIGH Voltage ¹	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
VIL	Input LOW Voltage ¹	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Volt- age ¹	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
VCC	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
IIH	Input HIGH Current			150			150			150			150	μΑ
IEE	Power Supply Current		55	66		55	66		55	66		65	78	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($V_{EE} = V_{EE}$ (min) to V_{EE} (max); $V_{CC} = V_{CCO} = GND$)

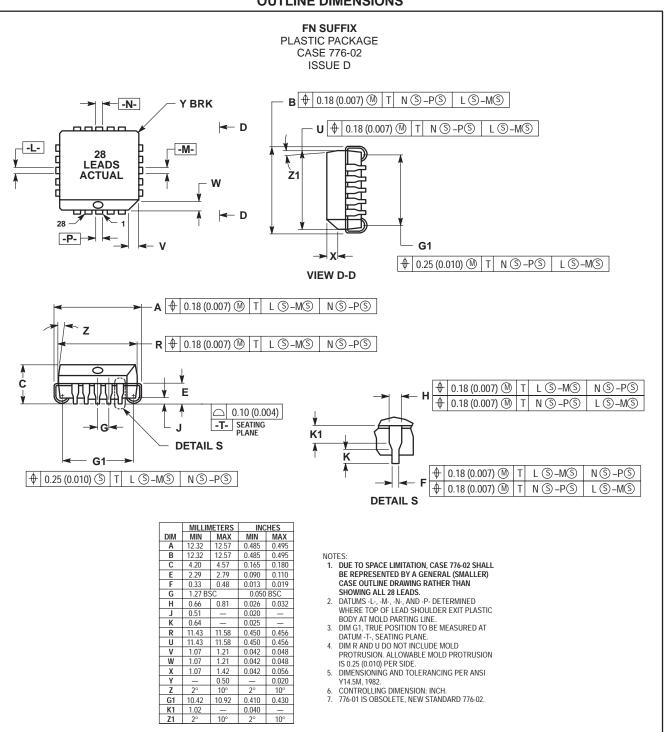
		-40°C			0°C			25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Unit	Condition									
^t PLH ^t PHL	Propagation Delay to Output IN (differential) IN (single-ended)	400 350		650 700	435 385		625 675	440 390		630 680	445 395		635 685	ps	Note 1 Note 2
^t skew	Within-Device Skew Part-to-Part Skew (Diff)			50 250			50 200			50 200			50 200	ps	Note 3
V _{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
VCMR	Common Mode Range	-1.5		-0.4	-1.5		-0.4	-1.5		-0.4	-1.5		-0.4	V	Note 5
t _r /t _f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).

The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

Vpp(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The Vpp(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.

V_{CMR} is defined as the range within which the V_I level may vary, with the device still meeting the propagation delay specification. The V_I level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).



OUTLINE DIMENSIONS

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MC100LVE111/D